

Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

Claims 1.-14. (Canceled)

15. (Original) A power-on/off reset circuit characterized by comprising a voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage, and outputs a first signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, and a new operational sequence being prevented when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted.

16. (Original) A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage, and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, a new operational sequence being prevented when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted, and an operation being immediately suspended when the power-supply voltage is equal to or lower than the third voltage.

17. (Original) A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal, the first signal being transmitted at the second voltage when a power-supply voltage rises and transmitted at the first voltage when the power-supply voltage drops, a time for a power-supply voltage to drop from the first voltage to the third voltage being longer than a predetermined operational sequence completion time.

18. (Canceled)

19. (Canceled)

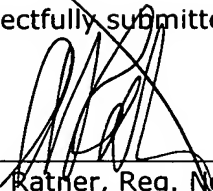
20. (Original) A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit including a voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, and preventing a new operational sequence when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than the first voltage or equal to or lower than the third voltage.

21. (Original) A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, preventing a new operational sequence when a power-supply voltage is equal to or lower than the voltage for the first signal to be transmitted, and immediately suspending an operation when the power-supply voltage is equal to or lower than the third voltage, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted or equal to or lower than the third voltage.

Respectfully submitted,


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Dated: March 10, 2004

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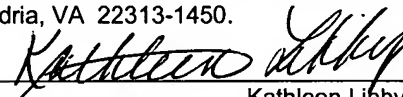
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March 10, 2004

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